WHAT IS CLAIMED IS:

1. A design verification system, comprising:

a first verification engine configured to model the operation of a first design of an integrated circuit and to assess the model's adherence to a property during N time steps of its operation;

means for recording and propagating the value of N;

a correspondence engine configured to determine the functional correspondence between the first design of the integrated circuit and a second design of the integrated circuit; and

responsive to the correspondence engine determining the functional correspondence of at least one node of the first design and a corresponding node of the second design, means for using the propagated value of N to reduce resources expended during subsequent analysis of the second design of the integrated circuit, wherein the subsequent analysis verifies the second design's adherence to the property during time steps greater than N.

2. The system of claim 1, wherein using the propagated value of N to reduce resources expended includes applying verification results achieved by the first verification engine to each of the nodes in the second design determined to have functional correspondence to a respective node in the first design.

3. The system of claim 2, wherein the correspondence engine is configured to determine functional correspondence between a node in the first design and a corresponding node in the second design includes creating a composite model including a composite node having a state determined by the state of the node in the first design and the respective node in the second design and monitoring the composite node, wherein assertion of the composite node negates the functional correspondence between the nodes in the first and second designs.

4. The system of claim 3, wherein the correspondence engine is further configured to simulate the new design using any debug traces for the old design and to simplify the composite model by eliminating any nodes in the new design that were hit during the simulation and removing any composite nodes corresponding to old design nodes for which no coverage was achieved.

5. The system of claim 4, wherein determining functional correspondence between a node in the first design and the corresponding node in the second design includes creating an EXOR node having a value of the exclusive or product of the node in the first design and the node in the second design when a common set of inputs are applied to the first and second designs.

6. The system of claim 4, wherein the node in the first design was shown to be hit by the first verification engine and further wherein determining functional correspondence between a node in the first design and the corresponding node in the second design includes creating an IMPLIED node that is asserted if and only if the node in the first design is ASSERTED and the corresponding node in the second design is NOT ASSERTED when a common set of inputs is applied to the first and second designs.

7. The system of claim 4, wherein the node in the first design was not shown to be hit by the first verification engine and further wherein determining functional correspondence between a node in the first design and the corresponding node in the second design includes creating an IMPLIED node that is asserted if and only if the node in the second design is ASSERTED and the corresponding node in the first design is NOT ASSERTED when a common set of inputs is applied to the first and second designs.

8. A computer program product for verifying the design of an integrated circuit, the program product comprising a computer readable medium, comprising:

first verification engine code means to model the operation of a first design of an integrated circuit and to assess the model's adherence to a property during N time steps of its operation;

code means for recording and propagating the value of N;

correspondence code means for determining the functional correspondence between the first design of the integrated circuit and a second design of the integrated circuit; and

code means, responsive to the correspondence engine determining the functional correspondence of at least one node of the first design and a corresponding node of the second design, for using the propagated value of N to reduce resources expended during subsequent analysis of the second design of the integrated circuit, wherein the subsequent analysis verifies the second design's adherence to the property during time steps greater than N.

9. The computer program product of claim 8, wherein the code means for using the propagated value of N to reduce resources expended includes code means for applying verification results achieved by the first verification engine to each of the nodes in the second design determined to have functional correspondence to a respective node in the first design.

10. The computer program product of claim 9, wherein the code means for reducing the resources expended includes omitting property violation checks when enumerating states of the second design of the integrated circuit for time steps less than N.

11. The computer program product of claim 8, wherein the code means for determining functional correspondence between a node in the first design and a corresponding node in the second design includes code means for creating a composite node having a state determined by the state of the node in the first design and the respective node in the second design.

12. The computer program product of claim 11, wherein the node in the first design was shown to be hit by the first verification engine and further wherein the code means for determining functional correspondence between a node in the first design and the corresponding node in the second design includes code means for creating an IMPLIED node that is asserted if and only if

the node in the first design is ASSERTED and the corresponding node in the second design is NOT ASSERTED when a common set of inputs is applied to the first and second designs.

13. The computer program product of claim 11, wherein the node in the first design was not shown to be hit by the first verification engine and further wherein the code means for determining functional correspondence between a node in the first design and the corresponding node in the second design includes creating an IMPLIED node that is asserted if and only if the node in the second design is ASSERTED and the corresponding node in the first design is NOT ASSERTED when a common set of inputs is applied to the first and second designs.

14. The computer program product of claim 11, wherein the code means for determining functional correspondence between a node in the first design and the corresponding node in the second design includes creating an EXOR node having a value of the exclusive or product of the node in the first design and the node in the second design when a common set of inputs are applied to the first and second designs.

15. A design verification system, comprising:

means for creating a composite of a first design of an integrated circuit and a second design of the integrated circuit;

wherein the composite design includes at least one correspondence node having a state determined by the state of a node in the first design and a corresponding node in the second design;

wherein the correspondence node exhibits an IMPLIED relation to the nodes in the first and second design, wherein the correspondence node is asserted when the node in the first design exhibits a state that was verified in a prior verification while the corresponding node in the second node does not; and

means for attempting to determine if the correspondence node is capable of being asserted.

16. The system of claim 15, wherein the correspondence node is asserted if and only if the node in the first design is TRUE and the corresponding node in the second design is NOT(TRUE).

17. The system of claim 15, wherein the correspondence node is asserted if and only if the node in the first design is NOT(TRUE) and the corresponding node in the second design is TRUE.

18. The system of claim 15, further comprising means for receiving a verification result from a first verification engine configured to model the behavior of at least a first node of the first design and means for applying the verification result to a first node of the second design if the correspondence node is determined to be incapable of being asserted.

19. The system of claim 18, wherein the first verification engine verifies the behavior of the first node of the first design for N timesteps.

20. The system of claim 19, wherein applying the verification result to the first node of the second design includes ignoring property checking of the first node of the second design during the first N time steps.